DESCRIPTION
The NE5050 is a modem for power line, coaxial cable, and twisted-pair communications. The modem incorporates features to overcome line impulse noise and line impedance modulation. The modem’s transmitter incorporates a Colpitts oscillator, positive logic, carrier-on/off switch, and a line driver. The receiver has an amplifier, a limiter, an amplitude detector, an amplitude modulation cancelling stage, an impulse filter, and an SR flip-flop. One NE5050 can be used to transmit and receive with Amplitude Shift Key (ASK) carrier-on/off modulation. With two NE5050s, Frequency Shift Key (FSK) modulation can be implemented. The transmitter input and the receiver output accept TTL or CMOS serial data.

FEATURES
- High receiver sensitivity — typ. 1.5mVRMS
- Receiver input overload protected for signals up to 70Vp-p
- High data rates — 300kbit/s ASK NRZ over twisted-pair
- The modem reaches the Nyquist limit of 1 bit per carrier cycle
- Has listen-while-talking for carrier sense multiple access/collision detect (CSMA/CD) networking capability
- Increased noise immunity with balance interstage ports for bandpass filtering
- Flexible oscillator can be made with LC tank (Colpitts), with crystal (Pierce), or accept external clock
- Signals are processed in real-time making this modem suitable for repeater/carrier translation applications

APPLICATIONS
- Twisted-pair communications
- Coaxial cable communications
- 120/277VRMS, 50 or 60Hz, power line communications

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
<th>ORDER CODE</th>
<th>DWG #</th>
</tr>
</thead>
<tbody>
<tr>
<td>20-Pin Plastic Dual In-Line Package (DIP)</td>
<td>0 to +70°C</td>
<td>NE5050N</td>
<td>0408B</td>
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<tr>
<td>20-Pin Plastic Small Outline Large (SOL) Package</td>
<td>0 to +70°C</td>
<td>NE5050D</td>
<td>0172D</td>
</tr>
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</table>

BLOCK DIAGRAM
### Power line modem

#### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>RATING</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply voltage</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>$V_{LOGIC}$</td>
<td>Logic supply voltage</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Ambient temperature range</td>
<td>0 to +70</td>
<td>°C</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction temperature range</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage temperature range</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>$P_{D\text{MAX}}$</td>
<td>Maximum power dissipation</td>
<td>700</td>
<td>mW</td>
</tr>
</tbody>
</table>

**NOTE:**
1. The power dissipation is based on $V_{CC} = 12\,\text{V}$, $T_J = +150^\circ\text{C}$, $TX_{OFF}$: $I_{CC} = 20\,\text{mA}$, $TX_{ON}$: $I_{CC} = 50\,\text{mA}$, $T_{JA} = 61^\circ\text{C/W}$ 20-pin plastic package.

#### DC ELECTRICAL CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $V_{CC} = 12\,\text{V}$, F carrier = 120kHz, data = NRZ, 50% duty cycle unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{HMIN}$</td>
<td>TX TTL input</td>
<td>TX$_{ON}$, Pin 19</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>$V_{ILMAX}$</td>
<td>TX TTL input</td>
<td>TX$_{OFF}$</td>
<td>300</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OLMAX}$</td>
<td>RX open-collector output</td>
<td>RX$<em>{ON}$, TX$</em>{ON}$, 100Ω load</td>
<td>100</td>
<td>mW</td>
</tr>
<tr>
<td>$I_{OLMAX}$</td>
<td>RX open-collector output</td>
<td>RX$_{OFF}$</td>
<td>220</td>
<td>mW</td>
</tr>
<tr>
<td>$I_{OLMAX}$</td>
<td>RX open-collector output</td>
<td>RX$_{ON}$, Pin 19</td>
<td>660</td>
<td>mW</td>
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<tr>
<td>$V_{OUT}$</td>
<td>RX data rate$^2$</td>
<td>$f_{OXR} = 120kHz, 500kHz$</td>
<td>DC</td>
<td>bit/s</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>RX data rate$^2$</td>
<td>$f_{OXR} = 120kHz, 500kHz$</td>
<td>1k</td>
<td>bit/s</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Carrier cycles per bit, TX and RX$^2$</td>
<td>1k</td>
<td>cycle</td>
<td></td>
</tr>
</tbody>
</table>

#### Broadband I/O ports, carrier

- **RX input sensitivity**: 1:1 input transformer
- **RX input signal level**: $V_{CC} \pm 35\,\text{V} = -25\,\text{V}, +51\,\text{V}$
- **RX input impedance**: Pin 20
- **RX line impedance modutation rejection**: 120HzAM 2V/20mV, 1bit/s
- **RX carrier frequency$^2$**: 0.1
- **PSRR**: RX power supply rejection ratio
- **Broadband port impedance**: RX$_{OFF}$ and TX$_{OFF}$
- **TX output signal level**: TX$_{ON}$, 100Ω load
- **TX driver output impedance**: TX$_{OFF}$
- **TX driver output impedance**: TX$_{ON}$
- **TX amplitude temperature drift**: External oscillator
- **TX amplitude temperature drift**: LC oscillator
- **TX output current capability**: TX$_{ON}$, Pins 15, 17
- **TX output THD (total harmonic distortion)**: TX$_{ON}$, LC oscillator
- **TX line drive amplifier BW**: At 6dB gain
- **TX carrier frequency$^2$**: DC
- **TX oscillator temperature drift**: Temperature range
- **TX oscillator initial frequency accuracy**: Sam LC tank
- **TX carrier feedthrough (leakage)**: TX$_{OFF}$

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ABBREVIATIONS:
TX = transmitter
RX = receiver

NOTES:
1. TX looped back to RX, data = 1kbit/s TTL, NRZ, 50% duty cycle ASK.
2. The NE5050 modem reaches the theoretical maximum data density for a given (fixed) carrier frequency. This limit is set by the maximum data bandwidth required before intersymbol interference occurs. The minimum specified limits are not tested in production. They are guaranteed by design.

PIN FUNCTION DESCRIPTION

Pin 1: \( +V_{CC} \)
For de-coupling \( V_{CC} \) to ground a 0.1μF capacitor must be placed close to Pin 1 and Pin 18.

Pin 2: \( C_{HPF} \)
High-pass filter, rejects 60Hz and its harmonics, rejects low frequencies, directing them to ground. Capacitor to ground: \( C_{HPF} = 10\text{nF for } f_{CXR} = 120\text{kHz and } C_{HPF} = 4.7\text{nF for } f_{CXR} = 300\text{kHz} \). The input amplifier provides a high-pass function: a +20dB/decade frequency response, with a DC attenuation of ~50dB. A frequency of 100kHz is amplified by +24dB. The ~3dB point of this high-pass filter is given by the equation:
\[
10^{0.4/(CHPF)}(F) = f_{-3dB} (\text{Hz})
\]

Pin 3: \( OUT_{1} \)
RX amplifier differential (+) output. Low impedance output. See Pin 6. Pin 3 can be connected to Pin 4 directly. A differential, bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{3dB} is controlled by the series resistors \( R_1 \) and \( R_2 \). An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 4, Pin 5: \( IN_{1}, IN_{2} \)
AM detector (±) inputs. High-impedance inputs = 27kΩ each. The require DC bias voltage from Pins 3 and 6 or around 4.5V. Pin 3 can be connected to Pin 4 directly. Pin 6 can be connected to Pin 5 directly. A differential bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{3dB} is controlled by series resistors. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 6: \( OUT_{2} \)
RX amplifier differential (-) output. Low impedance output. See Pin 3. Pin 6 can be connected to Pin 5 directly.

Pin 7, Pin 8: \( C_{DET} \)
Amplitude detector (±) output capacitor between Pins 7 and 8. \( t_{DET} \) is the time it takes for \( C_{DET} \) to charge from 0mV to 50mV, where 50mV is the detection threshold. The delay time, \( t_{DET} \), affects the receiver's jitter. \( t_{DET} \) is a term in a sum of delays, the sum being the total receiver delay, \( t_{D} \). See below in 'Receiver Delays' the relation between \( t_{D} \) and the maximum bit rate. The \( C_{DET} \) capacitor value is given by:
\[
C_{DET} (F) = t_{DET} (sec) / 10^5
\]

Pin 9: \( C_{AM} \)
Line impedance modulation rejection capacitor. A 0.1μF capacitor to ground provides about 4s of delay for the transition from receive data to standby. The \( C_{AM} \) value is determined in function of the receive string or in the preamble. It is a measure of the "readiness" of the receiver to switch from the "standby" mode to the "receive data mode" with no loss of leading bits. A low \( C_{AM} \) value will make the modem react faster (shorter delays) in both transition directions: from "standby" to "receive data" (incoming or departing messages) and from "receive data" to "standby" (absence of data traffic). Its value should be:
\[
C_{AM} (F) = 10\text{–}4 \text{bit rate [bits/s]}
\]

Pin 10: \( C_{IMP} \)
Impulse noise rejection capacitor. At 1kbit/s a 10nF capacitor to ground provides 350μs of delay and impulse rejection. This capacitor determines the receiver impulse noise immunity (transmission channel with non-Gaussian noise). \( t_{IMP} \) is the time it takes to ramp up or down the \( C_{IMP} \) voltage (the beginning of the ramp is delayed by \( t_{DE} \)). The shortest bit should last longer than the widest impulse. \( t_{IMP} \) is a term in a sum of delays, the sum being the total receiver delay, \( t_{D} \). See 'Receiver Delays' for the relation between \( t_{D} \) and the maximum bit rate. The \( C_{IMP} \) capacitor value is determined by the equation:
\[
C_{IMP} (F) = t_{IMP} (\text{s}) / 85\Omega
\]
The following equation determines \( t_{IMP} \):
Maximum rejected or expected impulse noise width \( t_{IMP} (\text{s}) < t_{IMP} (\text{s}) \)

Pin 11: RX Data Output
Open-collector RX output. RX data output.
\[
I_{OL\text{MAX}} = 5\text{mA} = V_{\text{LOGIC}} / R_{\text{PULL-UP}}
\]

Pin 12: \( C_{F0} \)
Oscillator feedback input. \( C_{F0} \) is 0 to 51pF capacitor between Pins 12 and 13. \( C_{F1} \) = capacitor between Pins 12 and GND. If the on-chip oscillator is used, \( C_{F1} \) may be omitted. If external oscillations are injected at Pin 13, \( C_{F0} \) must be removed and \( C_{F1} \) must be connected to GND. Grounding Pin 12 disables the oscillator.

Pin 13: Oscillator I/O
Colpitts LC oscillator tank, Pierce crystal oscillator, or external oscillator input.

On-chip LC oscillator — oscillator output. External oscillator tank present. Parallel LC components attached between Pins 13 and 14. \( C_{F0} \) attached between Pin 12 and Pin 13. A resistor between Pins 13 and 14 can decrease the oscillation amplitude to the desired level. Amplitudes above 2V peak may have THD > 2%. \( C_{F1} \) is not used. The amplitude varies with temperature; thermistor compensation recommended at Pin 16.

On-chip crystal oscillator — oscillator output. Two external capacitors in series, \( C_{13} \) and \( C_{14} \). \( C_{13} \) is connected to Pin 13 and \( C_{14} \) is connected to Pin 14. The external crystal is attached between Pin 13 and the connection of \( C_{13} \) and \( C_{14} \). An optional inductor \( L \), attached between Pins 13 and 14, tuned at the oscillation frequency.
frequency by C13 and C14 prevents oscillations at the crystal overtones. C30 and C31 are not used.

External oscillator — oscillator input. Parallel LC components attached between Pins 13 and 14 provide bias to Pin 13 and perform bandpass filtering. If a square wave is generated from a microprocessor by clock division, a series LC from the divider output to Pin 13 will perform additional bandpass filtering. C31 = 0.1μF is connected to ground. C20 is not used. If a sinusoidal wave is available, a 50Ω resistor may replace the parallel LC bandpass filter and a 0.1μF capacitor may replace the series LC bandpass filter. The amplitude is constant over temperature.

Pin 14: +VCC/2
Oscillator bias at +VCC/2. A 0.1μF de-coupling capacitor to GND is optional. Parallel LC components attached between Pins 13 and 14.

Pin 15: TX Carrier Output (NPN Transistor Base)
Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

NPN external Darlington transistor drive — Drives 1Ω loads.

NPN external transistor drive — 1Ω – 0.5W – R3 to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R3 between Pins 15 and 16 for 50Ω loads.

Pin 16: TX Line Drive Feedback
RFEEDBACK adjusts the driver amplifier gain. Minimum gain (RFEEDBACK = 0) is 2 (6dB). A thermistor can compensate the LC oscillator amplitude variation. R3 resistor (and NPN EB junction) to Pin 15. RFe resistor (and PNP EB junction) to Pin 17. The CDRIVE coupling capacitor is in series with the RD1VE resistor from Pin 16 to Pin 20. The RDRIVE value is the assumed line impedance. The CDRIVE impedance is 1/(2π fCRM CDRIVE).

Pin 17: TX Carrier Output (PNP Transistor Base)
Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

PNP external Darlington transistor — Drives 1Ω loads.

PNP external transistor drive — 1Ω – 5.0W – R5 to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R5 between Pins 16 and 17 for 50Ω loads.

Pin 18: Ground

Pin 19: TX Data Input
Transmitter TTL data input. Logic 1 will turn the transmit driver on, and sinusoidal carrier will be sent to the line from a low impedance source. Logic 0 will turn the driver off, to high output impedance.

Pin 20: RX Carrier Input
Receiver carrier input. Withstands an over-voltage of +VCC ±335V. DC bias connected through the line coupling transformer secondary to +VCC (Pin 1). The CDRIVE coupling capacitor is in series with the RD1VE resistor from Pin 16 to Pin 20.

DESCRIPTION OF OPERATION
The NE505 modem has been designed for transmitting and receiving control and data signals over the AC power lines, coaxial cables and twisted-pair cables. The modem overcomes line impulse noise and line impedance modulation. Two carrier modulation methods can be used: carrier on/off ASK, NRZ data and non-coherent FSK.

The power line is not an ideal medium for communication. The line noise, interference and losses are caused by: impulse noise, CW interference, line impedance modulation, and distribution transformer attenuation. NE5050 was designed to support both ASK and non-coherent FSK communications in this environment.

Listen-While-Talk
The IC modem is always in the receive mode, even when transmitting (it receives its own carrier). This capability permits remote RX and TX functionality testing for each system node. In the receive mode, the modem receives carrier signals from other transmitters. In the transmit mode, the modem transmits carrier to other receivers and receives its own carrier.

On-Chip Collision Detection
The listen-while-talk capability enables this IC to perform CSMA/CD (carrier-sense, multiple-access/collision detect) networks. Collision is detected when the local TX intends to transmit and the line is not clear.

In Dense Data Traffic
The RX data output (RXOUT) does not have time to go into the standby (lower power consumption, inverted logic) mode. In this case the RXOUT is in positive logic (carrier-on = 1, carrier-off = 0). A collision is detected at the local node when the local TX is on and the local RXOUT = 1. Collision: remote carrier present and detected. Abort local transmission. If, however, standby occurs (bursts of high-speed data) a proper value of CRAM will insure capture of all leading bits except for the first "10" transition.

In Rare Data Traffic
The RXOUT is in standby most of the time. In this case the RXOUT logic mode is inverted due to a designed-in offset present in the AM rejection and impulse filter circuits. A logic sequence from the local TX insures proper RX offset adjustment (preamble, the first "10" bits). The collision detection proceeds as in the dense data traffic case. The transition time from the last received bit "1" to the standby mode is proportional to the value of the AM rejection capacitor at Pin 9. For CRAM = 10nF, the "receive data" to "standby" transition occurs after 4 seconds from the last "1". Therefore, long strings of "0"s can be transmitted and received. The standby function may be disabled with proper bias at Pin 9 (external components).

TX-to-RX and RX-to-TX Switching Times
With the listen-while-talk capability the TX-to-RX and the RX-to-TX switching times have the meaning of TXON-to-TXOFF and TXOFF-to-TXON switching times, respectively. The TX-to-RX and RX-to-TX minimum switching times can be calculated from the maximum data rate. Since one bit can last a minimum of 3μs (NRZ ASK data), this may be considered the minimum switching time.

Data Rate
The maximum data rate is 300kbit/s NRZ ASK. This data rate was achieved on a twisted-pair cable with a 150kHz, 50% duty cycle square wave fro data. The data rate depends on the BPF (between Pins 3 – 4 and 5 – 6), on the AM detector capacitor for delay, CRDET (between Pins 7 and 8), on CRAM (Pin 9) for capture of leading bits, and on the desired impulse noise immunity for delay, CRIMP (Pin 10).
AC Line Coupling Network

One or two (120V or 240V and 277V AC RMS) coupling capacitors rated 600V are connected in series with the primary of a 1:1 transformer and connected to the AC line. The transformer secondary may be tuned to the carrier frequency by a capacitor (TOKO transformer, low data rates) or no secondary tuning capacitor for higher data rates (AIE Magnetics transformer). Two back-to-back zener diodes must be placed between Pins 1 and 20 for the IC transient protection (1N4744 or 1N6275). The transformer secondary carries DC bias current between Pins 1 and 20 of the IC. This coupling network itself attenuates to below the RX input sensitivity the 50 or 60Hz and their harmonic frequencies. In a coaxial cable application the transformer can be replaced with a coupling capacitor.

Receiver (RX)

The typical RX sensitivity is 1.5mVRMS. For less sensitivity, adjust the turn ratio of the coupling transformer or insert loss in the bandpass filter. The RX-only function can be implemented by not using the oscillator and by grounding the TX input. The maximum data rate is 300kbit/s. The power supply rejection ratio (PSRR) is 80dB for 60Hz and 120Hz. The RX is composed of the following blocks:

The Input Amplifier/Limiter limits its output signals to 1.2VPP-R. The maximum input carrier signal can be 70VPP-R. The gain is 24dB. The input amplifier highpass characteristic has the upper −3dB frequency internally fixed at 300kHz. The lower −3dB frequency is adjustable with the CHPF capacitor from Pin 2 to GND. For maximum RX sensitivity CHPF = 10nF at fCXR = 120kHz. A CHPF = 0.1μF value attenuates 60Hz by 50dB and 120Hz by 45dB.

The Bandpass Filter is differential RLC bandpass filter which can be connected from Pins 3, 6 to Pins 4, 5. The LC values are the same as the oscillator LC values (see Pins 13 and 14). The formulae relating the BW-3dB to the RLC values are:

\[
\frac{BW_{-3dB}}{ω_{CXR}} = \frac{1}{2 \cdot R} = \frac{1}{Q}
\]

\[
\frac{BW_{-3dB}}{ω_{CXR}} = \frac{1}{ω_{CXR} \cdot R} = \frac{1}{Q}
\]

\[
ω_{CXR} = 2 \cdot R \cdot f_{CXR}
\]

If no bandpass filter is required, connect Pin 3 to 4 and Pin 5 to 6 (R1 = R2 = 0Ω).

The Amplitude Detector is a Gilbert phase detector with a single differential input. The compared signals are always in phase and the demodulated output is a full rectified wave, function of the bias current, the carrier amplitude, and the collector load. The detected voltage is developed across a differential capacitive load between Pin 7 (+) and Pin 8 (−). DC offset is caused by the line impedance modulation.

The AM Rejection Circuit stabilizes the DC average value of the envelope by adding or subtracting a series voltage to the voltage of the detector capacitor. The AM rejection is 40dB at a modulation rate of 120Hz. The value of the AM rejection capacitor CAM (Pin 9 to GND) determines the transition times to and from receive data and standby.

The Slicing Comparator has current output and a fixed threshold of 50mV.

The Impulse Filter consists of a capacitor, CIMP, at the output of the comparator, from Pin 10 to GND. This capacitor is charged or discharged with constant current from the comparator, causing the voltage variation to be a constant slope in time. Narrow current impulses will not last long enough to fully charge or discharge the capacitor.

2VIMP Voltage Hysteresis provides a voltage interval in which the CIMP voltage ramps and in which both inputs to the SR flip-flop are zero.

The Flip-Flop is an SR type, with an open-collector transistor output at Pin 11. The transistor can switch a maximum load of 5mA.

Receiver Delays and Maximum Data Rate

The total receiver delay is a sum of delays, where tDET (sec) is the detector delay, tIMP (sec) is the impulse filter delay, and 2μs is the approximate receiver delay with no CDET and no CIMP:

\[
t_{0} (sec) = total
taker delay = t_{DET} (sec) + t_{IMP} (sec) + 2μs
\]

The maximum bit rate, in the no-return-to-zero, amplitude shift keying data format is determined by: Maximum bit rate MRZ ASK (bit/sec) < 1/td (sec−1)

NOTE: The CDET and CIMP values so calculated are for guidance and the user shall determine the optimal performance values in a range between 0.1 times to 10 times the calculated values (power line environment assumed). For twisted-pair or coaxial cables the calculated values are close to optimal. Based on power line applications made at 100kbits/sec and at 50kbits/sec, the CIMP/CDET capacitor ratios ranges from 1:0.1 to 1:1.

Transmitter, TX

The transmitter includes an oscillator, a line driver, and a drive switch.

The TTL Switch is a low power TTL gate that switches on/off the bias current for the line driver. A logic “1” at Pin 19 (TX/N) enables the line driver and carrier is being sent on the line. A logic “0” disables the driver.

The Oscillator is a differential transistor pair. It can be configured as a Colpitts LC oscillator, as a Pierce crystal oscillator, or used with external input (microprocessor clock divided to the carrier frequency). When the TX drive is off, the carrier leak is less than 90dBmO. Pin 18 can be used as input for an external oscillator. Grounding Pin 12 disables the oscillation process.

The Line Driver is a class AB push-pull stage with optional external complementary transistor pair for increased current capability. The TX output impedance is 40Ω in the off-state (receive mode) and less than 20Ω in the on-state (transmit mode). Note that in the transmit mode one receives its own signal. To increase the amplitude of the transmitter, add a feedback resistor in the driver amplifier feedback path at Pin 16.

By itself the NE5050 is capable of driving consumer line impedance of 50Ω (40mA peak/80mA non-repetitive), the THD being less than 2%. With complementary transistors, 10Ω industrial loads can be driven. With complementary Darlington transistors, 1Ω industrial loads can be driven.

One design objective was to provide the user with a flexible IC modem for residential as well as for industrial AC lines, for
Twisted-pair, and for coaxial cables. The IC modem can be used for control functions and data applications. Practical observations of power line noise point to a data rate upper boundary of 1kbit/sec. The main sources of interference are the light dimmers. Software for error correction can be used for improved error rates. Two system configurations can be implemented: an AM system and a non-coherent FSK system. The non-coherent FSK system can continue to transmit ASK data if the other channel is made unusable by CW interference. High-voltage transient protection and filtering are accomplished with user-selected external components.

Additional flexibility is provided by the chip architecture: one-IC real-time repeater, one-IC dual-frequency gateway, external oscillator input port, the listen-while-talk capability (CSMA/CD), immediate TX-to-RX switching, ASK and FSK, and ASK-multiplex single-frequency network.

The modem can be used for control systems and data applications in homes and other consumer environments and in industry.
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