820241 - DMD - Microelectronic Design

Coordinating unit: 295 - EEBE - Barcelona East School of Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering
Academic year: 2016
Degree: BACHELOR'S DEGREE IN INDUSTRIAL ELECTRONICS AND AUTOMATIC CONTROL ENGINEERING (Syllabus 2009). (Teaching unit Optional)
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ECTS credits: 6
Teaching languages: English

Teaching methodology

The teacher will show digital integrated circuit (chip) analysis and design procedures and how to configure commercial programmable logic devices (FPGAs and CPLDs) and some exercises to be solved by students will be proposed during the course.
In parallel, at the lab, the student will learn how to use electronic design computer tools to perform its own designs and to settle the learned concepts during lecture sessions.
A small design project on a digital electronic circuit will be also developed and experimentally verified using high level design tools (VHDL).

Learning objectives of the subject

To learn how to analyze and design electronic integrated digital circuits on applications specific circuits (ASIC) or standard programmable logic devices (PLD) using high level hardware description languages.
To learn how to analyze and design the basic elements that constitute a digital electronic circuit.
To learn how to use the tools for Electronic Design Automation (EDA) that are available on the market.

Requirements

To have completed the course on Digital Electronics and Microprocessors and Electronic Technology

Degree competences to which the subject contributes

Specific:
1. Design analogue, digital and power systems.

Transversal:
2. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.
3. EFFECTIVE USE OF INFORMATION RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.

Coordinator:
Cosp Vilella, Jordi
### Study load

<table>
<thead>
<tr>
<th></th>
<th>Hours large group:</th>
<th>45h</th>
<th>30.00%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total learning time:</td>
<td>150h</td>
<td></td>
<td></td>
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<tr>
<td>Hours medium group:</td>
<td>0h</td>
<td></td>
<td>0.00%</td>
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<tr>
<td>Hours small group:</td>
<td>15h</td>
<td></td>
<td>10.00%</td>
</tr>
<tr>
<td>Guided activities:</td>
<td>0h</td>
<td></td>
<td>0.00%</td>
</tr>
<tr>
<td>Self study:</td>
<td>90h</td>
<td></td>
<td>60.00%</td>
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### Introduction to Microelectronics

**Description:**
Introduction and basic concepts of microelectronic technology and design

**Related activities:**
None

**Specific objectives:**
To be introduced to microelectronic basics.

<table>
<thead>
<tr>
<th>Learning time:</th>
<th>5h</th>
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</thead>
<tbody>
<tr>
<td>Theory classes:</td>
<td>2h</td>
</tr>
<tr>
<td>Self study:</td>
<td>3h</td>
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</tbody>
</table>

### High Level Hardware Description of Integrated Circuits (VHDL)

**Description:**
The VHDL language and its application to integrated digital circuit design
- Concurrent statements
- Sequential statements
- Testbench generation
- Restriction files generation
- Digital design advanced concepts

**Related activities:**
Development of a digital design using the high level hardware description language VHDL and practical verification of its functionality on a programmable device (FPGA)

**Specific objectives:**
To learn how to design digital systems using high level hardware descriptions.

<table>
<thead>
<tr>
<th>Learning time:</th>
<th>54h 30m</th>
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<tbody>
<tr>
<td>Theory classes:</td>
<td>19h</td>
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<tr>
<td>Laboratory classes:</td>
<td>7h</td>
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<tr>
<td>Guided activities:</td>
<td>0h</td>
</tr>
<tr>
<td>Self study:</td>
<td>28h 30m</td>
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### Review of MOS Transistor Fundamentals

**Description:**
- MOS transistor models and basic concepts
- MOS transistor characteristic curves
- Modes of operation
- NMOS transistor vs PMOS transistor
- The current source

**Related activities:**
To obtain the current-voltage curve of type N and P MOS transistors by simulations and extract their most important parameters.

**Specific objectives:**
To know the basics of MOS transistors and to be able to use correctly these models in circuit design and analysis.

**Learning time:** 18h
- Theory classes: 4h
- Laboratory classes: 2h
- Self study: 12h

### The microelectronic Process

**Description:**
- Introduction
- Description of the VLSI microelectronic process
- The layout

**Related activities:**
To draw an elementary microelectronic circuit layout.

**Specific objectives:**
To know what the manufacturing process of CMOS integrated circuits is and understand its implications on the behaviour and performance of this kind of circuits.

**Learning time:** 10h
- Theory classes: 4h
- Self study: 6h
### The MOS Inverter

**Description:**
- CMOS inverter structure
- DC inverter behaviour
- Dynamic inverter behaviour

**Related activities:**
Design and verify the behaviour through simulations of a CMOS inverter.

**Specific objectives:**
To understand the behaviour of a CMOS inverter, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

<table>
<thead>
<tr>
<th>Learning time: 21h 30m</th>
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<tr>
<td>Theory classes: 6h</td>
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<tr>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>Self study: 13h 30m</td>
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### Static Logic Gates

**Description:**
- Description of NAND and NOR static gates
- DC behaviour of the NAND and NOR gates
- Dynamic behaviour of NAND and NOR gates
- AND-OR-INVERTER logic
- CMOS transmission gate

**Related activities:**
Design and verify the behaviour through simulations of a CMOS logic gate.

**Specific objectives:**
To understand the behaviour of a CMOS logical gate, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

<table>
<thead>
<tr>
<th>Learning time: 23h</th>
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<tbody>
<tr>
<td>Theory classes: 6h</td>
</tr>
<tr>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>Self study: 15h</td>
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Sequential Circuits

**Description:**
The RS latch
The level triggered latch
The edge triggered flip-flop

**Related activities:**
Design and verify the behaviour through simulations of a CMOS flip-flop.

**Specific objectives:**
To understand the behaviour of a CMOS flip-flop, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

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**Qualification system**

Midcourse exam: 10%; Final written test 25% Laboratory exercises: 25% Design project: 40%

**Regulations for carrying out activities**

It is required to have completed the laboratory exercise and bring the ID card or other identification on the day of testing.

**Bibliography**

**Basic:**

**Complementary:**